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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,108	01/05/2004	Richard William Earnshaw	550-506	1346

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EXAMINER	
WHITMORE, STACY	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 08/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,108	EARNSHAW ET AL.	
	Examiner	Art Unit	
	Stacy A. Whitmore	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-19* is/are rejected.

7)☒ Claim(s) *11 and 20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/328,420.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

FINAL ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claims 1-3, 5-7, 10, 12-13, 15, and 18-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Baxter (US Patent 6,018,624).

2. As for the claims Baxter discloses the invention as claimed, including:

1. and 19 (Original) A method (and apparatus for) of modeling an integrated circuit, said method comprising the steps of :
(i) generating (memory for storing) a circuit component model including signal transitions with a set of associated delays and rules for a given implementation of said integrated circuit [abstract; PLD simulation model; timing characteristics; col. 2, line 41 – col. 3, line 13; col. 4, lines 11-42; rules are part of the circuit description and PLD simulation model];

(ii) (a delay calculator) calculating signal delays for signal transitions within said circuit component model using a delay calculator and a subset of said set of associated delays and rules [col. 2, line 41 – col. 3, line 13]; and
(iii) searching said circuit component model to identify signal transitions corresponding to signal transitions with associated signal delays as calculated by said delay calculator [col. 2, line 41 – col. 3, line 13]; and
(iv) (modifying logic for) modifying said circuit component model for identified matching signal transitions with said delays calculated by said delay calculator and said set of associated delays and rules [abstract; col. 2, line 41 – col. 3, line 13; the new simulation model is generated and based on matching].

2. (Original) A method as claimed in claim 1, wherein if said searching does not identify a matching signal relationship within said circuit component model for a signal transition and delay calculated by said delay calculator, then said signal transition and delay is passed directly to said circuit component model [col. 2, line 41 – col. 3, line 13].

3. (Original) A method as claimed in claim 1, wherein said integrated circuit includes a macrocell which is modeled within said circuit component model other than by a details of individual circuit components [col. 11, lines 32-36].

5. (Original) A method as claimed in claim 1, wherein, if said circuit component model includes a plurality of a signal transitions that match a signal transition and delay calculated by said delay calculator, then said signal transition and delay calculated by said delay calculator is used to modify all of said plurality of signal transitions within said circuit component model [col. 2, line 41 – col. 3, line 13].

6. (Original) A method as claimed in claim 1, wherein if said signal transitions and delays calculated by said delay calculator include a plurality of signal transitions and delays that match a signal transition within said circuit component model, then that signal transition and delay calculated by said delay calculator that most specifically matches said signal transition within said circuit component model is used to modify said signal transition within said circuit component model [col. 2, line 41 – col. 3, line 13; col. 12, lines 35-39].

7. (Original) A method as claimed in claim 1, wherein if signal transitions and

delays calculated by said delay calculator include a signal transition and delay that is more specifically defined than any signal transition within said circuit component model, then the most specifically matching signal transition within said circuit component model is modified with said signal transition and delay [col. 2, line 41 – col. 3, line 13; col. 12, lines 35-39].

10. (Original) A method as claimed in claim 1, wherein said set of associated delays and rules within said circuit component model includes associated condition parameters and said signal transitions and delays calculated by said delay calculator do not include condition parameters [col. 11, lines 13-31].

12. (Original) A method as claimed in claim 10, wherein modified delay values for all of said condition parameters are inferred from said calculated delay using relative differences between said delays within said circuit component model [col. 2, line 41 – col. 3, line 13; col. 12, lines 35-39].

13. (Currently Amended) A method as claimed in claim 1, wherein at least one of said associated set of delays and rules includes edge direction parameters [col. 11, lines 18-20, edge direction may be the hold or setup due to the hold and setup being associated with the direction of the edge of a signal].

15. (Original) A method as claimed in claim 1, wherein said circuit component model is a netlist model with associated timing and rule data [col. 2, netlist model].

18. (Original) A method as claimed in claim 1, wherein said step of modifying is responsive to constraint data specifying instructions for how said modification should be performed [col. 6, lines 59-66].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made

to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claim 4,8-9, 12, 14, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Baxter (US Patent 6,018,624) in view of Earnshaw, R., et al., "Challenges in Cross-development".

4. As for the claims, Baxter discloses the invention substantially as claimed, including the method and apparatus for modeling an integrated circuit and cited above in the rejection of claims 1, 3, 7, 10, 15, and 19.

Baxter does not specifically disclose
4. (Original) A method as claimed in claim 3, wherein said macrocell is a microprocessor core.
8. (Original) A method as claimed in claim 1, further comprising the step of generating an audit log representing the steps taken.
9. (Original) A method as claimed in claim 7, further comprising the step of generating an audit log representing the steps taken and wherein said modification of said most specifically matching signal transition within said circuit component model with said more specifically defined signal transition and delay is recorded in said audit log.
14. (Original) A method as claimed claim 1, wherein said delay calculator outputs results as a standard delay format file [].
16. (Original) A method as claimed in claim 15, wherein said associated timing and rule data is a standard delay format file.
17. (Original) A method as claimed in claim 16, wherein said step of modifying modifies said standard delay format file.

Earnshaw discloses wherein said macrocell is a microprocessor core [pg. 33, left hand side – The ARMulation framework section – ARM processor core]; the step of

generating an audit log representing the steps taken [pg. 33, fig. 5, transaction control; pg. 34, left hand side discussion of transaction control]; the step of generating an audit log representing the steps taken and wherein said modification of said most specifically matching signal transition within said circuit component model with said more specifically defined signal transition and delay is recorded in said audit log [pg. 33, fig. 5, transaction control; pg. 34, left hand side discussion of transaction control]; and a standard delay format file [pg. 31, right hand side].

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Baxter and Earnshaw because utilizing Earnshaw's core, transaction control comprising an audit log, and SDF file would have provided Baxter's system with a single chip solution for a programmable device, and using standard files for debug (audit) and using a SDF for describing external and not internal signals for a processor core to provide a total single-chip package [see Earnshaw pg. 28 and 31].

5. Claims 11 and 20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art of record fails to disclose either singularly or in combination a method of modeling a circuit comprising at least the step of wherein different condition parameters of a signal transition within said circuit component model have different delays associated with them and said delay calculator calculates a delay for only one condition parameter.

7. Applicant's arguments filed June 6, 2006 have been fully considered but they are not persuasive.

8. In the remarks, applicant argues in substance:

A: Baxter does not disclose (ii) (a delay calculator) calculating signal delays for signal transitions within said circuit component model using a delay calculator and a subset of said set of associated delays and rules [col. 2, line 41 – col. 3, line 13]; and
B: Baxter does not disclose (iii) searching said circuit component model to identify signal transitions corresponding to signal transitions with associated signal delays as calculated by said delay calculator [col. 2, line 41 – col. 3, line 13]; and
C: Baxter does not disclose (iv) (modifying logic for) modifying said circuit component model for identified matching signal transitions with said delays calculated by said delay calculator and said set of associated delays and rules [abstract; col. 2, line 41 – col. 3, line 13; the new simulation model is generated and based on matching].
D: Baxter does not disclose using a subset of the set of associated delays and rules for the given implementation of the IC.

9. Examiner respectfully disagrees for the following reasons:

As for argument A: A: Baxter does disclose (ii) (a delay calculator) calculating signal delays for signal transitions within said circuit component model using a delay calculator and a subset of said set of associated delays and rules [col. 2, line 41 – col. 3, line 13; col. 6, col. 7, lines 6-8, col. 8, lines 8-15, col. col. 11, lines 1-62, col. 12, lines 25- 51 – The PLD model is modified (a new model generated) by back annotation with timing values from target technology, via specification delays, derived, and net delays, in which all or a portion of the PLD model is modified, so as to include a subset of associated delays and rules].

As for argument B: Baxter does disclose (iii) searching said circuit component model to identify signal transitions corresponding to signal transitions with associated signal delays as calculated by said delay calculator [col. 2, line 41 – col. 3, line 13; col. 2, line 41 – col. 3, line 13; col. 6, col. 7, lines 6-8, col. 8, lines 8-15, col. col. 11, lines 1-62, col.

12, lines 25- 51 – The PLD model is modified by back annotation with timing values from target technology, via specification delays, derived, and net delays, in which all or a portion of the PLD model is modified, so as to include a subset of associated delays and rules; using derived, and net delays (calculated values for timing associated with elements), elements from the original PLD model are replaced with new ones to meet a target technology, the back annotation requires that the corresponding elements are replaced with target elements with similar or matching characteristics].

As for argument C: Baxter does disclose (iv) (modifying logic for) modifying said circuit component model for identified matching signal transitions with said delays calculated by said delay calculator and said set of associated delays and rules [abstract; col. 2, line 41 – col. 3, line 13; col. 2, line 41 – col. 3, line 13; col. 2, line 41 – col. 3, line 13; col. 6, col. 7, lines 6-8, col. 8, lines 8-15, col. col. 11, lines 1-62, col. 12, lines 25- 51 – The PLD model is modified by back annotation with timing values from target technology, via specification delays, derived, and net delays, in which all or a portion of the PLD model is modified, so as to include a subset of associated delays and rules; using derived, and net delays (calculated values for timing associated with elements), elements from the original PLD model are replaced with new ones to meet a target technology, the back annotation requires that the corresponding elements are replaced with target elements with similar or matching characteristics].

As for argument D: The argument that Baxter does not disclose using a subset of the set of associated delays and rules for the given implementation of the IC is irrelevant because the claim language does not disclose this particular limitation as argued.

10. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stacy A. Whitmore whose telephone number is (571) 272-1685. The examiner can normally be reached on Monday-Thursday, alternate Friday 6:30am - 4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Stacy A Whitmore
Primary Examiner
Art Unit 2825

SAW
August 7, 2006